DESIGN ISSUES FOR BUS SWITCH SYSTEMS IN DEEP SUB-MICRO METRIC CMOS TECHNOLOGIES

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ABSTRACT

The high data-rate communication channels represent one of the most *power-aware* design problem, trying to decrease energy consumption maintain acceptable some other performance constraints. In this context, the *bus-switch* mechanism represents a novel and efficient bus encoding approach for low-power data off-chip buses. It is based on tentatively encoding, clustering, reordering and encoding a wide data buses according to a reordering pattern and a fixed coding function. Unfortunately, the hardware complexity limits the field of application in high capacity off-chip buses, where dynamic energy saving dominates the encoding power consumption. The paper addressed the design issues for bus-switch systems, employing industrial MOSFET models up to 90nm. Additionally, we evaluated the basic hardware resources: area, latency and power dissipation. Results indicated how future CMOS technologies enhance the bus switch's field of application.

KEY WORDS

Bus transfer, Encoding, Power demand, Very-large-scale integration

1 Introduction and Background

The increased demand for low-energy-consuming and high-data-rate interconnections in digital embedded systems have been encouraging the development of encoding schemes for address and data buses. The activity reduction in address buses [11] [3] [4] exploits the fact that consecutive fetch addresses mostly present a small Hamming distance, due the instruction locality during program execution. Moreover, the address space can be partitioned in different working zones which are used to make the memory access with a reduced bus [5]. Adaptive techniques trace the address bus for a given program, choosing the best encoding scheme in those applications showing low level of address sequentiality (Beach Code) [2]. Additionally, different encoder/decoder models have been proposed for a general approach to the problem [1] [7] (Information-Theoretical code). As a general result, while statistical approaches assume data statistics known in advance, such assumption does not hold in many applications, where the more general adaptive techniques are preferable. The on-chip bus encoding for low-power seems to do not represent effective power reduction for future generation silicon-based SoC at high data rate. Instead, the off-chip bus interconnections represent the major concerns, where novel approaches seem to be promising. In this context, the bus-switch mechanism (BS) represents one of the most meaningful approaches for reducing dynamic power consumption. It is based on tentatively encoding, dividing a large bus into identical clusters. The clusters have been reordered and encoded using a common reordering pattern and a fixed coding function. The authors in [6] demonstrated how this approach implied a convenient VLSI implementation for reducing dynamic energy dissipation in a high-capacity off-chip bus. The minimal bus capacitance for BS' convenient employment is strictly related to the encoder's power consumption. The road map for semiconductor CMOS technology quickly decreases the energy consumptions, enabling faster VLSI implementations [8]. Instead, the off-chip technology specifications cannot follow the CMOS road map basically for signal integrity purposes. For this reason, the sub-micro metric CMOS technology will enable a more conveniently BS utilization as minimal parasitic bus line capacity. This paper explored the design issues translating the BS HDL description in recent sub-micro metric CMOS technologies (from ST Microelectronics). We derived the basic VLSI implementation parameters: area, energy, max frequency and minimum bus capacitance for iterative and full parallel BS architectures [6]. We inferred the performance of the BS approach in very sub-micro metric technologies: 45nm and beyond. Results confirmed how the full parallel architecture permits the best timing and energy performance, when area does not represent a relevant constraint. The paper follows this organization. Section 2 illustrated and extended the bus-switch mechanism and design issues. Section 3 illustrated the effects of technology scaling in BS design. Section 4 illustrated the main VLSI implementation parameters for different BS architectures. Lastly, section 5 concluded the work.

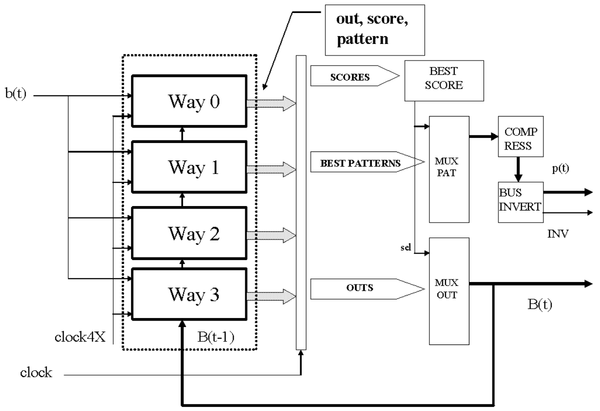

Figure 1. The 2 pipe stages BS encoder (Type III): 32-lines 4-Way and 16 optimized patterns

2 The Bus Switch Mechanism

In principle, the Bus Switch technique can be logically expressed as a four-step process:

1. A large bus is divided into several identical clusters of M (cluster depth) lines each.
2. Each M-line bus is coded by swapping the input lines using a particular *reordering pattern*
3. A tentative data encoding is obtained by applying to the swapped M lines a fixed *coding function.*
4. The process is repeated M! times from step 2 until the optimal reordering pattern is found, that minimizes the output switching activity in the encoded data of the whole bus.

In the following a formal definition of the process is given. Let $b(t)$ be input data word to the bus encoder and $B_{opt}(t)$ the encoded data word on the bus, at clock cycle t. The single bits of any M-bit data word $x(t)$ will be indicated as $x(t)(0), x(t)(1), , x(t)(M-1)$.

Definition 1 *A reordering pattern $p(t)$ is an ordered set of M indices $i_0 \dots i_{M-1}$, associated with clock cycle t. Given a data word $x(t)$, the swap operator S_w with reordering pattern p is a combinational logic function producing a swapped data word $y(t) = S_w(x(t), p(t))$, such that :*
y(t)(0) = x(t)(i_0);y(t)(1) = x(t)(i_1);. . . ,
y(t)(M-1) = x(t)(i_{M-1}).

As an example, if $p(t)$ = "1,2,3,0" and $x(t)$ = "0100", then $S_w(x(t), p(t))$ = "1000". Note that each reordering pattern $p(t)$ has a unique inverse $p^{-1}(t)$, such that $x(t) = S_w\big(S_w\big(x(t), p(t)\big), p^{-1}(t)\big)$. For instance if $p(t) =$ "1, 2, 3, 0" than $p^{-1}(t) =$ "3, 0, 1, 2"

Definition 2 *A coding function is a combinational logic function producing a data word $B(t)$, applying swapping to $b(t)$ and employing any other words resulting from input or output observation.*

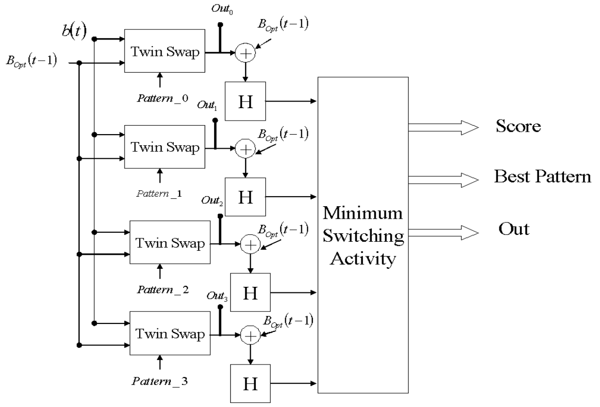

Figure 2. The Full Parallel Single Way

Definition 3 *The optimal reordering pattern $p_{opt}(t)$ is the reordering pattern that minimizes the switching activity (score see fig.1) $H[B_{opt}(t-1) \oplus B(t)]$, where H is the Hamming distance from previous transmission $B_{opt}(t-1)$ and the coding function result, varying the reordering pattern.*

Table 1 illustrates different coding/decoding functions, for the proposed low-power bus encoding approach. Table 2 shows the switching activity savings employing Bus Switch and prior approaches: Bus Invert (BI) [10] and Adaptive Partial Bus Invert (APBI) [9] . Results indicated how the simple bus reordering (Type I) does not guarantee a clear convenience with traditional approaches. The BS approach, where reordering and coding have been combined, permits performance better than bus-invert and adaptive versions. The efficiency of coding could be easily justified since the bus reordering de-correlates the input stream $b(t)$. Encoding functions, whose XOR operator receives strongly un-correlated processes, gives the best activity savings. The process $B(t)$ increases its correlation in Type III much better than other analyzed functions. However, other encoding functions permit similar activity savings implying different VLSI design implementation. For instance:

$$B(t) = b(t) \oplus S_w\big(B_{opt}(t-1), p^{-1}(t)\big) \qquad (1)$$

decreases area and power at similar switching activity reduction compared to BS-III (Average 15.85%). The BS encoder employs different parallel *ways* [6] devoted to tentatively encoding in a sub-set of trials (Fig. 1). The authors in [6] illustrated the iterative BS VLSI implementation. However, each way can select the best reordering pattern in a parallel manner as illustrated in fig.2. This last solution seems to conveniently represent the best circuit, when area overhead does not represent a critical design parameter. The major design issue for reducing energy dissipation in a BS encoder, concerns the reordering pattern set reduction by either on-line or off-line analysis. This approach does not significantly affect switching activity performance, enhancing the BS convenience as minimal para-

Circuit	Coding Function	Decoding Function
BS Type I	$B(t) = S_w\big(b(t), p(t)\big)$	$b(t) = S_w\big(B_{opt}(t), p^{-1}(t)\big)$
BS Type II	$B(t) = S_w\big(b(t), p(t)\big) \oplus S_w\big(b(t-1), p^{-1}(t)\big)$	$b(t) = S_w[\big(S_w\big(b(t-1), p^{-1}(t)\big) \oplus B_{opt}(t)\big), p^{-1}(t)]$
BS Type III	$B(t) = S_w\big(b(t), p(t)\big) \oplus S_w\big(B_{opt}(t-1), p^{-1}(t)\big)$	$b(t) = S_w[\big(S_w\big(B_{opt}(t-1), p^{-1}(t)\big) \oplus B_{opt}(t)\big), p^{-1}(t)]$

Table 1. Different coding and decoding functions

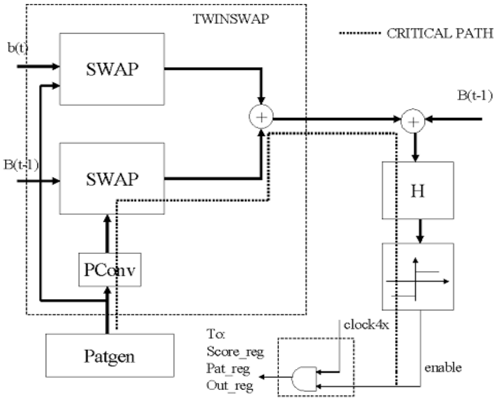

Figure 3. BS-Type III Critical Path (Iterative VLSI)

sitic capacitance:

$$C_{min} = \frac{2}{\alpha \cdot Vdd^2} \cdot E_{encoder} \cdot \frac{1}{N + EL} \qquad (2)$$

The N-line bus operates at frequency 1/T with a signal level V_{dd}. EL represents the BS' extra lines, α the average switching activity reduction and $E_{Encoder}$ the estimated BS energy consumption.

3 The effects of technology scaling in bus-switch design

The very large scale integration systems take benefit of the bus switch approach, employing recent sub micro-metric technologies. In this context, the proposed approach is able to encode digital information at high data-rate, preserving a satisfactory toggling savings. The main advantage of BS approach can be summarized as follows:

- Differently from Information-Theoretic codes, BS represents an adaptive approach, which does not require the prior statistical knowledge of input traffic. This issue makes convenient the proposed solution in general purposes SoC.
- Differently from prior approaches, the BS mechanism introduces light activity losses increasing the bus' length. This issue implies the use of the proposed technique in high data-rate transmission.
- The proposed method provides an iterative metric (H) evaluation for minimizing the switching activity. The metric could be easily modified for solving different problems concerning buses (e.g. crosstalk noise in on chip-buses)

Test	BS-I	BS-II	BS-III	BI	APBI
LaTeX	7.22%	12.65%	20.38%	7.78%	6.70%
Spice	4.96%	13.99%	20.51%	10.65%	10.21%
Gcc	6.36%	13.11%	17.51%	9.06%	8.37%
JPeg	14.27%	17.29%	15.61%	10.02%	6.54%
MP3	14.46%	17.46%	16.70%	10.27%	6.39%
AVI	5.32%	2.26%	16.24%	0.04%	6.12%
Average	8.76 %	12.79 %	17.82 %	7.97 %	7.38 %

Table 2. Convenience of BS approach, with respect to known algorithms (32-line bus, cluster depth 4 and full reordering pattern set).

We discussed how the semiconductor road map provides a technology scaling more rapidly with respect to the off-chip electrical specifications. Intel recently announced the possibility to reach 5nm MOSFET, following the process paradigms from 90nm and below. In this scenario, the impact of nano-technology on the bus switch design represents a major concern. The process of technology scaling operated with MOSFET channel length reduced by a factor β. This assumption implies the decrease of power and increase power density of β^2. Additionally, the effect of leakage current is dominating at 90-65 nm. In this context, the challenge of convenient off-chip bus encoding for reducing the dynamic power will be represented by the hardware / activity savings / data rate trade-offs. The clustered bus invert (CBI) and adaptive partial bus invert represented the most competitor bus encoder. In the point of view of future sub-micrometric technologies and high data rate transmission demand, the bus switch mechanism should be preferred for the following reasons:

Name	Description	Used Patterns
BS-6WAYS	Iterative arch.	24
BS-4WAYS	Iterative arch.	16
BS-2WAYS	Iterative arch.	8
BS-FULL24	Full Parallel arch.	24
BS-FULL16	Full Parallel arch.	16
BS-FULL 8	Full Parallel arch.	8

Table 3. Different BS variants

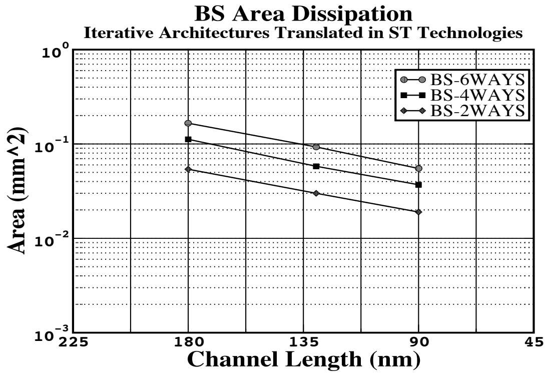

Figure 4. Iterative BS Area Dissipation

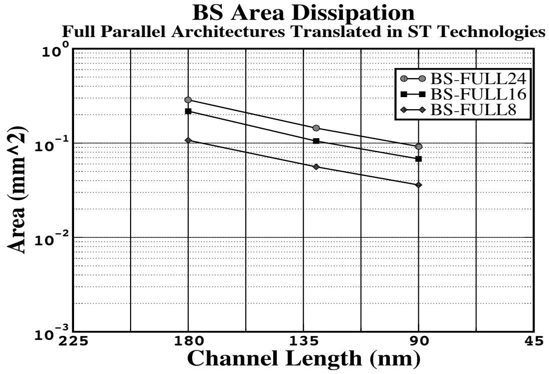

Figure 5. Full Parallel BS Area Dissipation

- At high data rate, CBI employed too much additional lines compared to BS at similar switching activity performance. Instead, BS' extra lines depend on used reordering patterns only.

- APBI requires additional memory and its VLSI implementation is comparable of a sub-optimal BS-encoder. This technique becomes un-effective at high data rate.

We concluded the road map for convenient BS passes through a sensible reordering pattern set reduction by an effective on-line or off-line analysis.

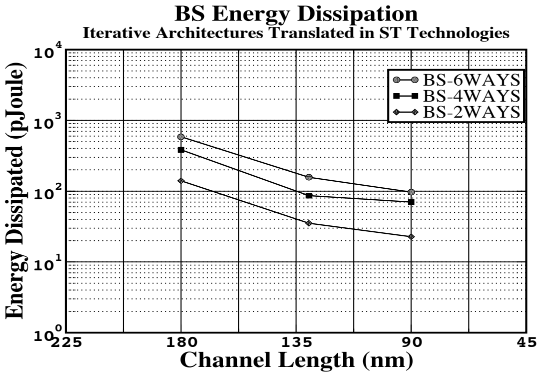

Figure 6. Iterative BS Energy Dissipation

4 Simulation Results

The BS architectural description (Verilog) has been translated in different industrial CMOS technologies from ST Microelectronics. A prior off-line analysis selects a variable number of used reordering pattern set, describing different VLSI circuit alternatives (Table 3). We started from 180nm low-leakage (year 2001) until 90nm high threshold voltage (today). We evaluated the area, energy and minimum latency for both iterative and full parallel architecture. The former circuit requires a secondary faster clock (clock4X, see fig.1) for the iterative encoding. Additionally, starting from a preliminary static timing analysis (STA, fig. 3), several timing optimizations have been pursued respect to the original BS [6]. The Hamming distance block, who counts the transitions by adder trees, employed carry-save adder implementations. Table 4 illustrated how this circuit reduces the Hamming block's latency, saving the 1.2% of the overall area. Additionally, as future researches for increase the max operative frequency, the massive use of multiplexer suggested the employment of full-custom box units [6] . Finally, we controlled the single way dynamic power, gating the clock4X in the iterative architecture. Results indicated:

- Area dissipations exponentially decrease in both iterative and full parallel architecture (fig. 4 and 5).

- Energy dissipation is much controlled in the full parallel architecture (fig 6 and 7). This energy estimation does not include the clock4X buffering at layout level.

- The clock gating is much effective in 180nm iterative circuit (fig. 6). The full-parallel corresponding architecture dissipates a lot of power (fig. 7).

- The max operative bus frequency reaches 300 MHz in 90nm and full parallel circuit. This result permits to operate BS encoding very close to the maximum core speed (fig.8 and 9).

- The minimum bus capacitance for convenient BS relive for the increased leakage current from 90nm as dominate contribution to total power. Additionally, the full parallel architecture provides the best capacity performance (fig 10 and 11).

- Results at 65nm confirmed exponential area reduction, with un-satisfactory max allowed bandwidh and minimal bus capacitance compared to 90nm. These issues have been confirmed in preliminary (no silicon) SoC implementations in 65nm at ST.

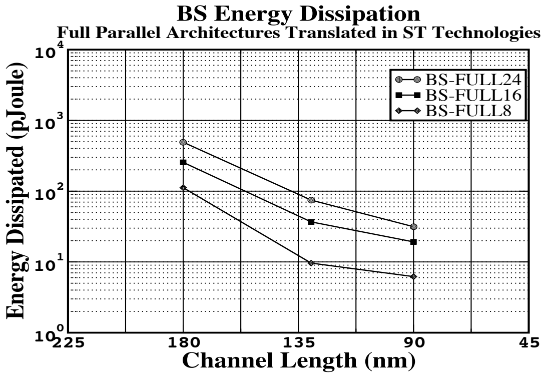

Figure 7. Full Parallel BS Energy Dissipation

As far as the minimum capacitance is concerned, we evaluated this theoretical parameter beyond the industrial CMOS at 90nm. In particular we evaluated the exponential regression for 8 patterns set both iterative (eq.3 BS-2WAYS) and full parallel solutions (eq.4 BS-FULL8):

$$C_{min}\big(L\big) = 0.16465 \cdot e^{0.020547 \cdot L} \quad (pF) \tag{3}$$

$$C_{min}\big(L\big) = 0.01192 \cdot e^{0.03314 \cdot L} \quad (pF) \tag{4}$$

We expected a minimal capacity at 45nm 0.415 pF and 0.052 pF for iterative and full parallel architectures respectively. The total balance of average energy saving per bus cycle is therefore:

$$E_{saved} = 0.5 \cdot \alpha \cdot C_{Bus} \cdot V_{dd}^2 - E_{overhead} \tag{5}$$

Where α represents the switching activity reduction and $E_{overhead}$ the encoder's energy dissipation; the total energy saving percentage is expressed by the ratio:

$$E_{\%} = \frac{\big(0.5 \cdot C_{Bus} \cdot V_{dd}^2 - E_{saved}\big)}{\big(0.5 \cdot C_{Bus} \cdot V_{dd}^2\big)} \cdot 100.0 \tag{6}$$

Sub-Module	Latency Original BS	Latency New BS
Swap Unit	0.78 ns	0.88 ns
H (Hamming)	1.71 ns	1.54 ns
PConv	0.65 ns	0.60 ns
Threshold Unit	0.37 ns	0.50 ns
Patgen	1.18 ns	1.13 ns
Network Delay	0.05 ns	0.05 ns
Other	0.26 ns	0.30 ns

Table 4. Static Timing Analysis (90nm CMOS, 20ns bus clock), comparing BS4X [6] and new version

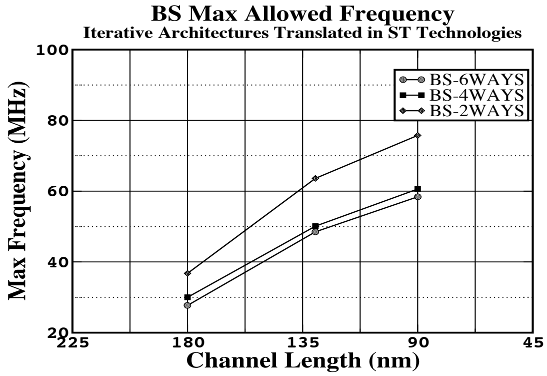

Figure 8. Iterative BS Max Allowed Frequency

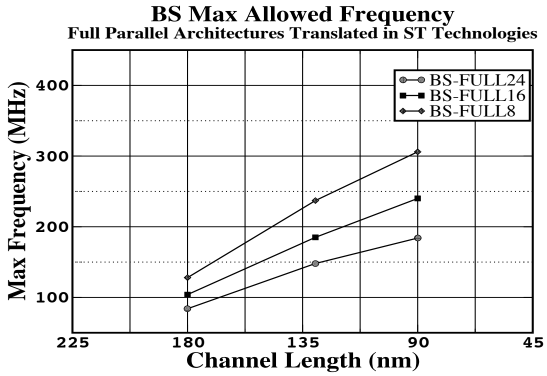

Figure 9. Full Parallel BS Max Allowed Frequency

A value of E% lower than 100% means that the BS is effective in reducing the total energy consumed per bus cycle, while E% greater than 100% means that the bus capacitance is so small that the energy overhead of the encoder dominates and the BS technique is inappropriate. Finally, fig.12 showed the BS 3X-4X bus line capacitance trade off, translating the RTL architectural description in 90nm CMOS process. A 12pF bus line capacitance divides the BS3X and BS4X convenience regions.

5 Conclusion

The paper presented the main VLSI parameters, concerning the implementation of a bus switch encoder in different CMOS industrial technologies. We expected an exponential area reduction, while the corresponding energy and minimum bus capacitance reduced their effects since an increasing leakage current. We confirmed the full parallel architecture introduced the best operative performances (capacitance and max frequency) when area does not represent a critical constraint. Since the static energy contribution, the major performance issues can be pursued by an effective on-line or off-line analysis for reducing the

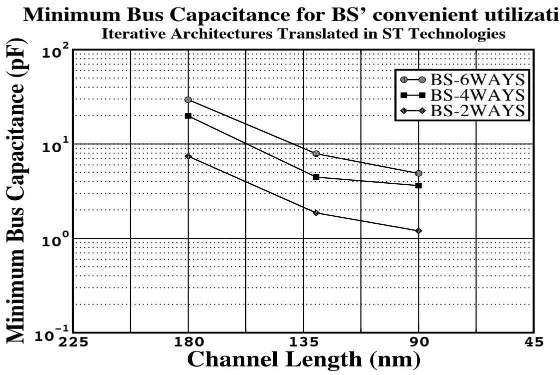

Figure 10. Iterative BS Minimum Bus Capacitance

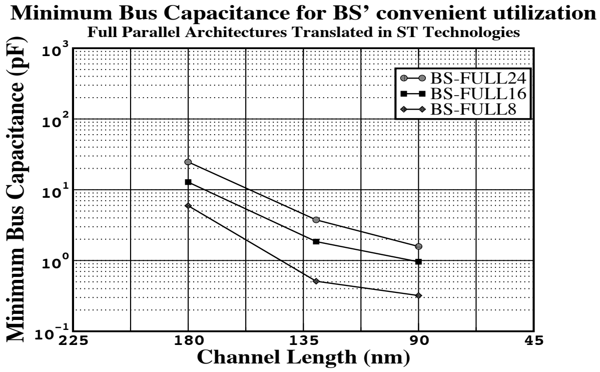

Figure 11. Full Parallel BS Minimum Bus Capacitance

set of reordering pattern. The paper also presented the expected minimum capacitance, by an exponential regression of the implementation data. Additionally, we suggested the BS3X architecture until 12pF bus line capacitance. Result confirmed how the bus switch systems take benefit for the future CMOS technologies, increasing the proper field of application.

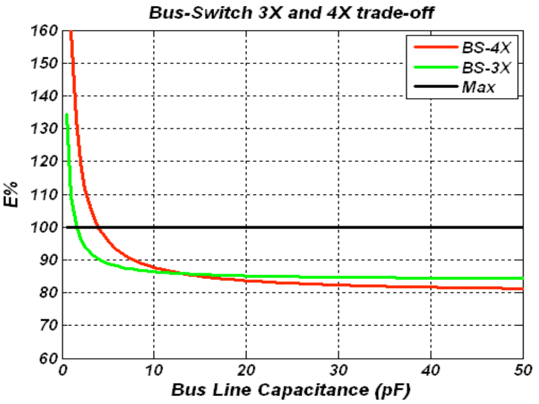

Figure 12. Bus-Switch 3X-4X trade-off (24-line bus, BS-Type III, full pattern set, CMOS=90nm and V_{dd}=2.5V)

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